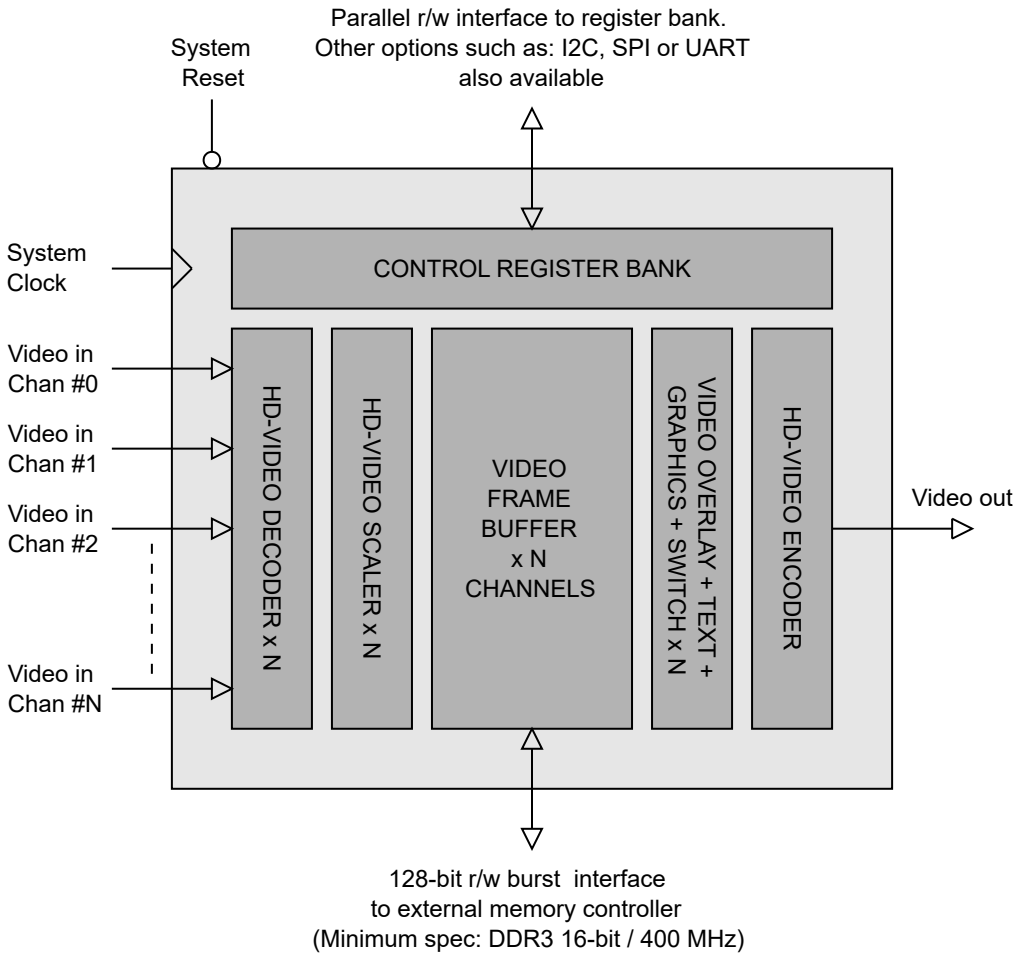
Block Diagram (simplified)

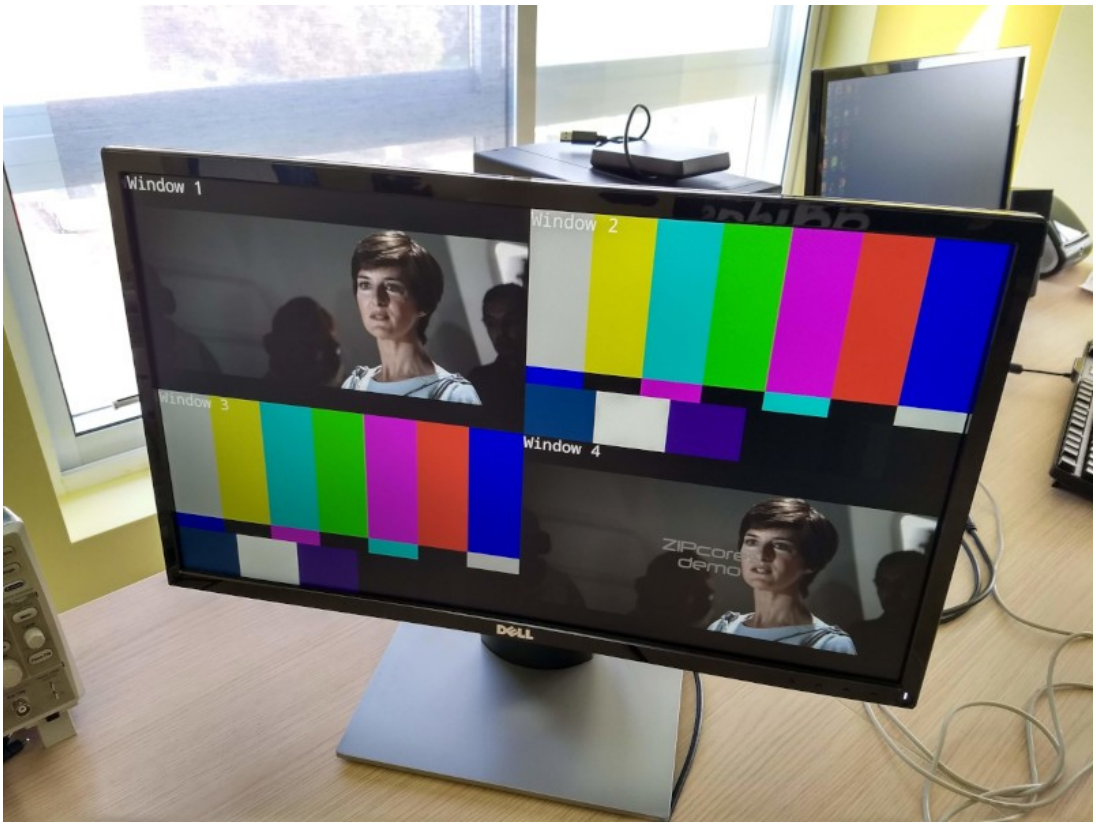


General description

This brief specification describes the operation of the HD Multi-window Video Processor (evaluation) IP Core. The IP Core is provided as a netlist in either EDIF, Verilog or VHDL formats.

The evaluation demo accepts 4 x standard HD720p60 video inputs and 1 x video output comprised of 24-bit RGB 8:8:8 pixel data, vsync, hsync, data enable and a 74.25 MHz pixel clock. The four video inputs are scaled-down into four separate video windows to present a quad-tiled display. The demo also generates a text overlay in the corner of each tiled window (Window1, Window2, Window3, etc ..) and a 50% alpha blended image that reads ‘ ZIPcores demo’ in the bottom right tile.

In addition, the IP Core requires a simple generic memory interface to allow the incoming video streams to be buffered in an external DDR3 memory. The only other signals necessary are a 150 MHz system clock and a system reset. All clock signals are asynchronous relative to each other. Any minor differences in frequency and/or phase are controlled by the internal frame buffer. The photo on the following page demonstrates a typical bench setup with the output video driving a standard COTS monitor via the HDMI port.



Pinout descriptions (VHDL entity declaration)

```
-- System signals
sys_clk         : in  std_logic;  -- 150 MHz
sys_reset       : in  std_logic;  -- active low

-- Video in #0
vin0_clk        : in  std_logic;  -- 74.25 MHz
vin0_rgb        : in  std_logic_vector(23 downto 0);
vin0_vsync      : in  std_logic;
vin0_hsync      : in  std_logic;
vin0_de         : in  std_logic;

-- Video in #1
vin1_clk        : in  std_logic;  -- 74.25 MHz
vin1_rgb        : in  std_logic_vector(23 downto 0);
vin1_vsync      : in  std_logic;
vin1_hsync      : in  std_logic;
vin1_de         : in  std_logic;

-- Video in #2
vin2_clk        : in  std_logic;  -- 74.25 MHz
vin2_rgb        : in  std_logic_vector(23 downto 0);
vin2_vsync      : in  std_logic;
vin2_hsync      : in  std_logic;
vin2_de         : in  std_logic;

-- Video in #3
vin3_clk        : in  std_logic;  -- 74.25 MHz
vin3_rgb        : in  std_logic_vector(23 downto 0);
vin3_vsync      : in  std_logic;
vin3_hsync      : in  std_logic;
vin3_de         : in  std_logic;
```

```
-- Video out
vout_clk        : in  std_logic;  -- 74.25 MHz
vout_rgb        : out std_logic_vector(23 downto 0);
vout_vsync      : out std_logic;
vout_hsync      : out std_logic;
vout_de         : out std_logic;

-- External memory read/write interface
mem_rw          : out std_logic;
mem_wdata       : out std_logic_vector(127 downto 0);
mem_addr        : out std_logic_vector(31 downto 0);
mem_addr_val    : out std_logic;
mem_addr_rdy    : in  std_logic;
mem_rdata       : in  std_logic_vector(127 downto 0);
mem_rdata_val   : in  std_logic );
```

System signals

The only system signals required are the 150 MHz system clock (*sys_clk*) and the active low (asynchronous) system reset (*sys_reset*). The system clock is used for general internal processing functions. The system reset can be asserted to reset the IP Core to initial conditions.

(Note that after the input video streams and clocks are stable, the system reset ***must*** be asserted for at least two system clock cycles in order for the IP Core to sync and lock correctly to the incoming video streams).

Control Register Bank

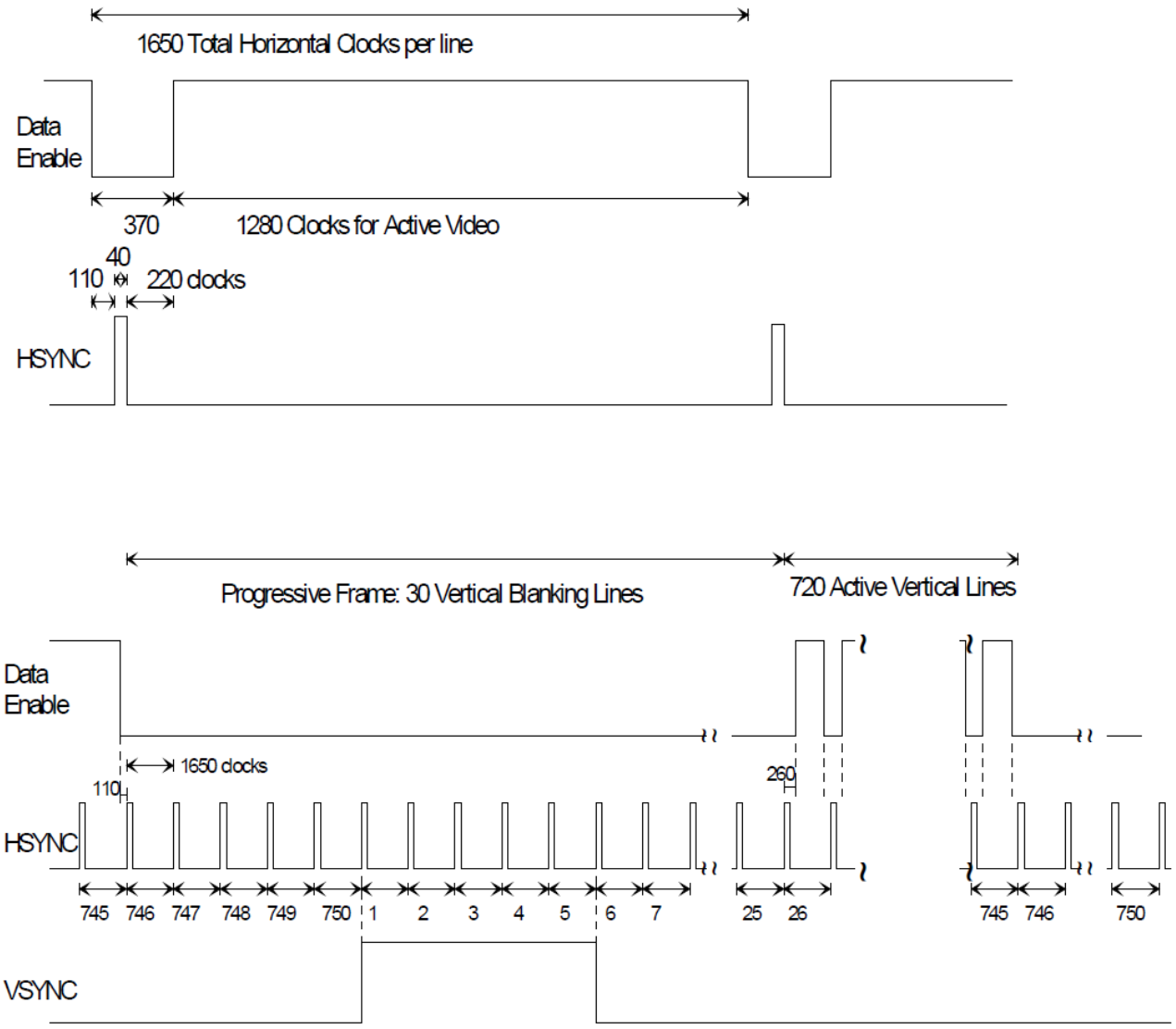
The control register bank is not used in the evaluation version of the IP Core. All functionality is fixed as the design is for demo purposes only. In a full implementation then the register bank may be used to control things such as video scaling, text and graphics overlays, dynamic zoom and movement of video windows.

There are various options for programming the register bank including a simple MCU-style parallel interface as well as UART, SPI and I2C options. Please contact us with your requirements and we can modify the design accordingly.

Video Inputs and Outputs

The 4 x video inputs and the 1 x video output is configured for a standard HD1280x720p60 video format stream with a 74.25 MHz pixel clock. The video timing information is defined in the following CEA/VESA timing parameters and timing waveforms:

	Horizontal timing (pixels)	***Vertical timing (lines)***
Visible area	1280	720
Front porch	110	5
Sync pulse	40	5
Back porch	220	20
Whole line/frame	1650	750



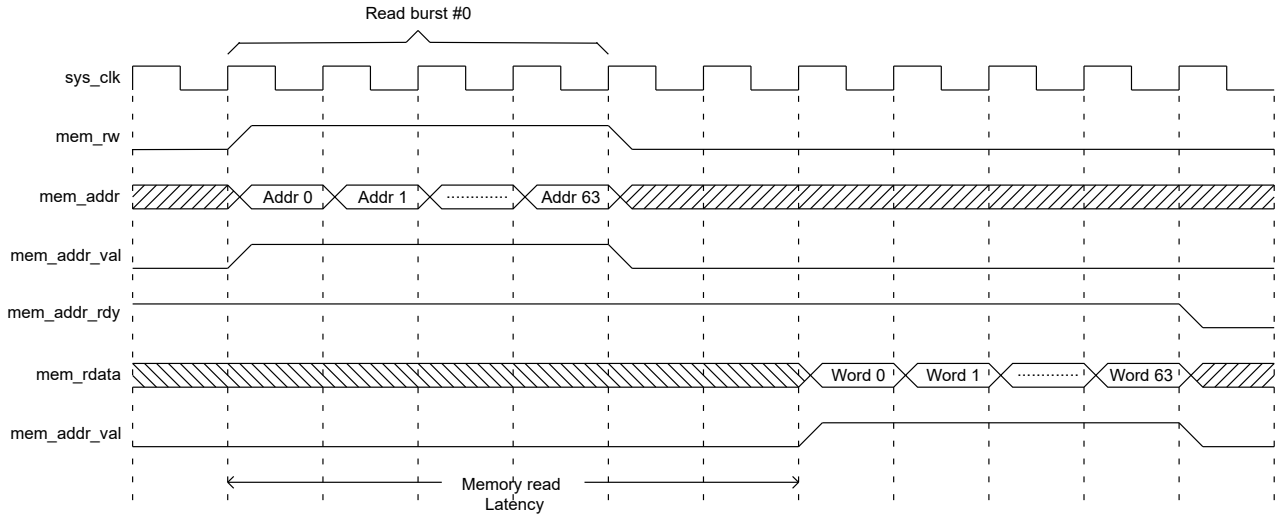
Timing Parameters for HD1280x720p @ 59.94/60 Hz

(Taken from CEA-861-D spec.)

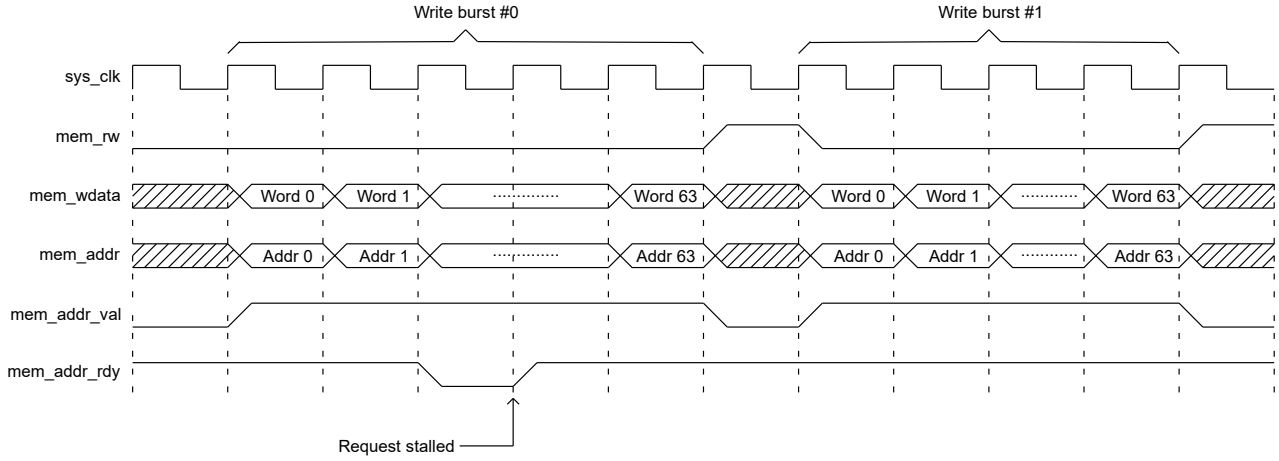
Generic Memory Interface

The timing diagrams below show a series of read and write bursts to memory. Each read or write burst is a request of 64 x 128-bit words. The addresses are guaranteed to be sequential within a burst.

Note that the *mem_addr_valid* signal and the *mem_addr_rdy* signal form a 'handshake' that controls the flow of data. Data is transferred on a rising clock edge when both these signals (valid and rdy) are high. If necessary, the downstream interface may stall a burst request by asserting *mem_addr_rdy* low. This is demonstrated in the second timing diagram.



Memory read request



Back-to-back memory write requests (showing one cycle stall in the first burst)

(Note: In order to support the memory interface requirements of the demo, then it is recommended that the external DDR3 memory is at least 16-bits wide running at 400 MHz or better. In addition, the size of the external memory should be at least 64 Mbytes in order to buffer the video correctly).