Key Design Features

- Synthesizable, technology independent VHDL Core
- Signed fixed-point or integer input
- 32-bit floating-point output
- Configurable word and fraction width up to 32 integer bits and 23 fraction bits
- IEEE 754 compliant
- High-speed fully pipelined architecture
- 2 clock-cycle latency

Applications

- Floating-point pipelines and arithmetic units
- Floating-point processors
- Interfacing between floating-point and fixed-point number systems

Pin-out Description

Pin name	*I/O*	*Description*	*Active state*
clk	in	Synchronous clock	rising edge
en	in	Clock enable	high
fixed_in [dw-1:0]	in	Signed fixed-point or integer input in [dw fw] format	data
ieee_out [31:0]	out	Floating-point output in IEEE 754 format	data

Generic Parameters

Generic name	*Description*	*Type*	*Valid range*
dw	Fixed-point word width	integer	2 ≤ dw ≤ 32
fw	Fixed-point fraction width	integer	0 ≤ fw ≤ 23 (fw < dw)

Block Diagram

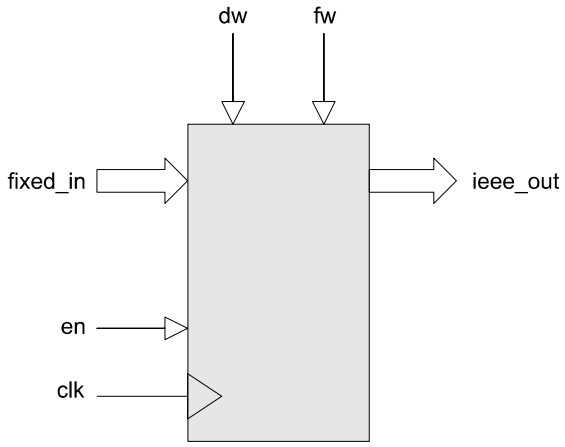
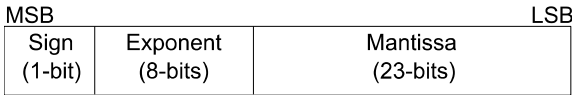


Figure 1: Fixed-point to 32-bit Floating-point converter

General Description

FIXED_TO_IEEE (Figure 1) is a high-speed fully pipelined conversion unit that accepts a signed fixed-point number as input and generates a 32-bit bit floating-point number at the output. The output number is based on the IEEE 754 standard with the bits arranged in the following format:



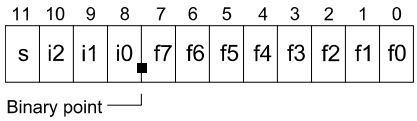
The real number representation of the floating-point number may be calculated as:

$$Value = -1(S) * 2^{(E-127)} * 1.\mathrm{M}$$

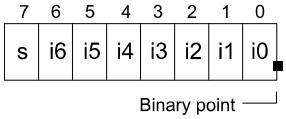
The fixed-point format is configured using the generic parameters *dw* and *fw*. The value *dw* specifies the width of the input word and *fw* specifies the number of fraction bits.

The input may be specified as either a signed fixed-point number or a signed integer. If a signed integer is preferred, then *fw* must be set to 0. In all cases *dw* must be at least 2 bits and *fw* must be less than *dw*.

As an example, consider a 12-bit fixed-point format with 8 fraction bits. The generic parameters would be set to: dw = 12, fw = 8. In this example the input word would be arranged as follows:



Alternatively, consider the case where the input format is an 8-bit signed integer. Setting dw = 8 and fw = 0, the input word would be:



All values are sampled on the rising clock-edge of *clk* when *en* is high. The function has a 2 clock-cycle latency.

Functional Timing

Figure 2 demonstrates the conversion of two fixed-point numbers. The first number is 0x80D and the second is 0x7C0 which represent the real numbers -7.95 and 7.75 respectively. The generic parameters have been set to: dw = 12, fw = 8. The results are available two clock cycles later.

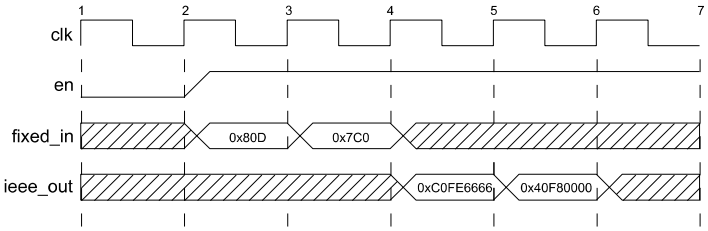


Figure 2: Fixed-point [12 8] format to floating-point conversion

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	Description
fixed_to_ieee.vhd	Top-level component
fixed_to_ieee_bench.vhd	Top-level test bench

Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. fixed_to_ieee.vhd
2. fixed_to_ieee_bench.vhd

The VHDL testbench instantiates the top-level component and the user may modify the generic parameters *dw* and *fw* as required

The simulation must be run for at least 2 ms during which time the 'fixed_to_ieee' component will receive an input stimulus of randomized fixed-point numbers.

The simulation generates two text files called : *fixed_to_ieee_in.txt* and *fixed_to_ieee_out.txt.* These files respectively contain the input and output values captured during the test.

Synthesis

The source file 'fixed_to_ieee.vhd' is the only file required for synthesis. There are no sub-modules in the design.

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx Virtex 5 and the Altera Stratix III series of FPGA devices. The lowest and highest speed grade devices have been chosen in both cases for comparison. Trial synthesis results are shown with the generic parameters set to: dw = 32, fw = 23.

Resource usage is specified after Place and Route.

VIRTEX 5

Resource type	Quantity used
Slice register	77
Slice LUT	364
Block RAM	0
DSP48	0
Clock frequency (worst case)	220 MHz
Clock frequency (best case)	280 MHz

STRATIX III

Resource type	Quantity used
Register	79
ALUT	301
Block Memory bit	0
DSP block 18	0
Clock frequency (worse case)	251 MHz
Clock frequency (best case)	322 MHz

Revision History

Revision	Change description	Date
1.0	Initial revision	09/05/2008
1.1	Updated synthesis results in line with minor source code changes	21/09/2011