

Key Design Features

- Synthesizable, technology independent VHDL Core
- Function $y = a * b$
- Input values as signed or unsigned numbers
- Output values as signed or unsigned numbers
- Configurable data width and pipeline depth
- High-speed fully pipelined architecture

Applications

- Fixed-point mathematics
- Fundamental building block in all digital processing functions

Pin-out Description

Pin name	I/O	Description	Active state
clk	in	Synchronous clock	rising edge
en	in	Clock enable	high
a_in [dw-1:0]	in	Input value #1	data
b_in [dw-1:0]	in	Input value #2	data
product [dw*2 - 1:0]	out	Output product	data

Generic Parameters

Generic name	Description	Type	Valid range
dw	Input data width	integer	≥ 1
levels	Number of pipeline stages	integer	≥ 1
use_signed	Use signed or unsigned arithmetic	boolean	TRUE/FALSE

General Description

PIPE_MULT (Figure 1) is a general purpose multiplier with a configurable data width and configurable number of pipeline stages. Input values are accepted as either signed or unsigned numbers depending on the generic setting *use_signed*. Equally, output values are either signed or unsigned depending on the same setting.

The number of pipeline stages may be programmed using the generic parameter *levels*. By changing this value, a multiplier may be generated which trades off latency against maximum attainable clock frequency.

Values are sampled on the rising clock-edge of *clk* when *en* is high. The function has a clock-cycle latency which is equal to the number of pipeline levels.

Block Diagram

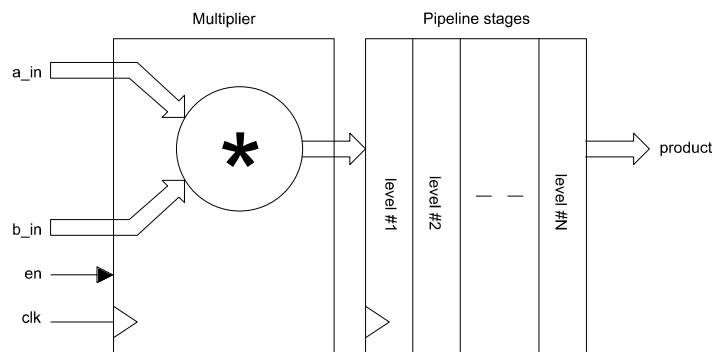


Figure 1: Pipelined multiplier architecture (conceptual model)

Functional Timing

Figure 2 demonstrates the computation of: $a_in * b_in$, where $a = 0xA92F$ (-22225 in decimal) and $b = 0x712C$ (28972 in decimal). In this example, the parameters have been set to $dw = 16$, $levels = 3$, $use_signed = true$. The result, $0xD99ED314$ (-643902700) has a latency of 3 clock cycles.

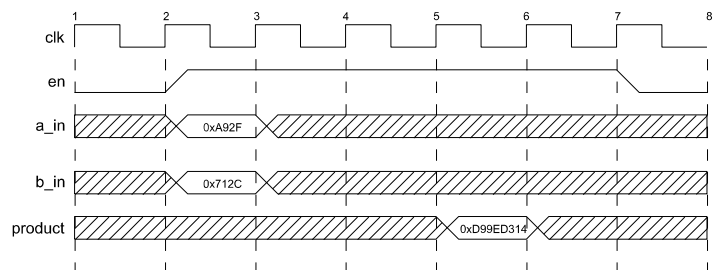


Figure 2: Calculation of $a * b$

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	Description
pipe_mult_reg.vhd	Pipeline register block
pipe_mult.vhd	Top-level block
pipe_mult_bench.vhd	Top-level test bench

Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. pipe_mult_reg.vhd
2. pipe_mult.vhd
3. pipe_mult_bench.vhd

The VHDL testbench instantiates the multiplier component and the user may modify the generic parameters as required. The simulation must be run for at least 2 ms during which time the multiplier will be driven with a randomized sequence input values. The test terminates automatically.

The simulation generates two text files called: *pipe_mult_in.txt* and *pipe_mult_out.txt*. These files respectively contain the input and output data samples captured at the interfaces during the test.

Figure 3 shows the results of the multiplier used to implement the function $f(x) = x^2$. Results are shown for the first 1000 samples.

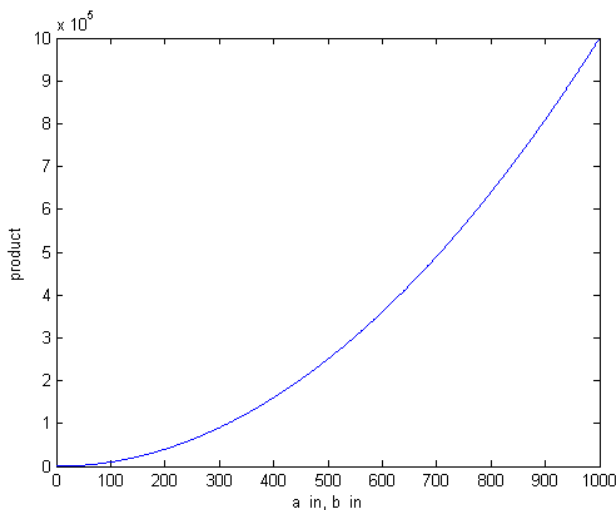


Figure 3: Plot of test results for function: $f(x) = x^2$

Synthesis

The source files required for synthesis and the design hierarchy is shown below:

- pipe_mult.vhd
- pipe_mult_reg.vhd

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx Virtex 5 and the Altera Stratix III series of FPGA devices. The lowest and highest speed grade devices have been chosen in both cases for comparison.

Synthesis results are shown with the generic parameters set to: $dw = 32$, $levels = 5$, $use_signed = true$.

Note that increasing the number of pipeline levels will increase the maximum attainable clock frequency (up to a point) for a given multiplier data width.

Resource usage is specified after Place and Route.

VIRTEX 5

Resource type	Quantity used
Slice register	49
Slice LUT	17
Block RAM	0
DSP48	4
Clock frequency (worst case)	502 MHz
Clock frequency (best case)	627 MHz

STRATIX III

Resource type	Quantity used
Register	68
ALUT	6
Block Memory bit	256
DSP block 18	4
Clock frequency (worse case)	368 MHz
Clock frequency (best case)	500 MHz

Revision History

Revision	Change description	Date
1.0	Initial revision	22/07/2008