

### Key Design Features

- Synthesizable, technology independent VHDL Core
- 32-bit floating-point arithmetic
- IEEE 754 compliant<sup>1</sup>
- High-speed fully pipelined architecture
- 5 clock-cycle latency

### Applications

- Floating-point pipelines and arithmetic units
- Floating-point processors

### Pin-out Description

Pin name	I/O	Description	Active state
clk	in	Synchronous clock	rising edge
en	in	Clock enable	high
v1 [31:0]	in	Input operand 1 in IEEE 754 format	data
v2 [31:0]	in	Input operand 2 in IEEE 754 format	data
vout [31:0]	out	Output result in IEEE 754 format	data

### Functional Specification

Operand v1	Operand v2	Result
Standard IEEE 754	Standard IEEE 754	if $ v1 + v2  \leq \text{MaxFloat}$ then result is: $v1 + v2$ If $ v1 + v2  > \text{MaxFloat}$ then result is: $\pm \text{Inf}$ If $ v1 + v2  < \text{MinFloat}$ then result is: $\pm 0$
NaN	Anything	NaN
$\pm \text{Inf}$	$-v1$	NaN (E.g. $-\text{Inf} + \text{Inf}$ )
$\pm \text{Inf}$	Standard IEEE 754	$[\text{sign}(v1)] \text{Inf}$

### Block Diagram

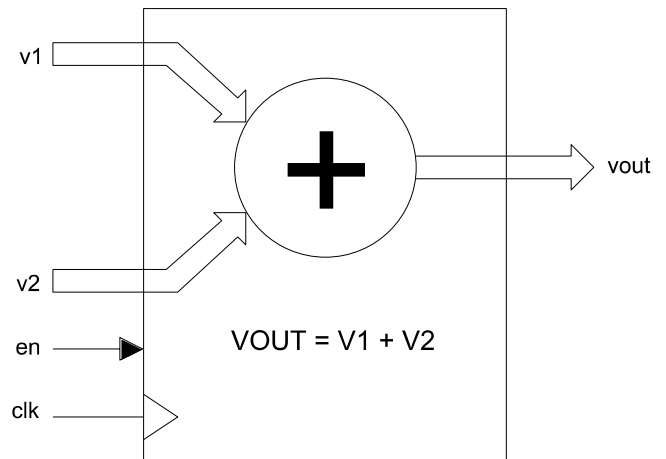


Figure 1: 32-bit floating-point adder

### General Description

IEEE\_ADD (Figure 1) is a high-speed fully pipelined 32-bit floating-point adder based on the IEEE 754 standard. The arrangement of the 32-bit floating-point number is summarized below:



All input and output values comply with the IEEE 754 specification, a real number being calculated as:

$$\text{Value} = -1(S) * 2^{(E-127)} * 1.M$$

There are two exceptions to the IEEE 754 specification. The first being that denormalized numbers are treated as zero throughout the implementation, and the second being that symmetric arithmetic rounding is employed (round half-up).

Other points to note are that NaN is always generated as the value 0xFFC00000. The maximum floating-point value that may be represented is 0x7F7FFFFF or 0xFF7FFFFF (MaxFloat). The minimum floating-point value that may be represented is: 0x00800000 or 0x80800000 (MinFloat). This means that a real number lies in the range:

$$2^{-126} \leq \text{Value} \leq 2^{127}(2-2^{-23})$$

All values are sampled on the rising clock-edge of *clk* when *en* is high. The function has a 5 clock-cycle latency.

<sup>1</sup> Some minor features diverge from the IEEE 754 specification

## Functional Timing

Figure 2 demonstrates the addition:  $0x40010000 + 0x40407000 = 0x40A04000$  (or  $2.0010 + 3.0068 = 5.0078$  in real numbers). The result has a latency of 5 clock cycles.

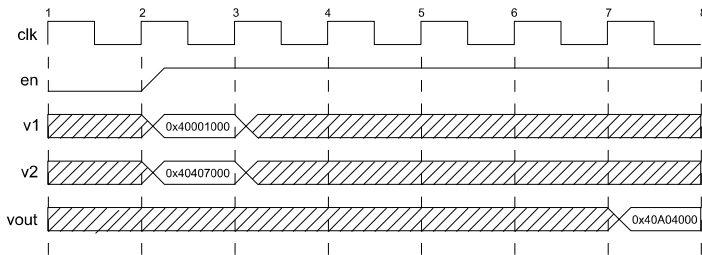


Figure 2: Addition of two floating-point numbers

## Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	Description
ieee_add.vhd	Top-level block
ieee_add_bench.vhd	Top-level test bench

## Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. ieee\_add.vhd
2. ieee\_add\_bench.vhd

The simulation must be run for at least 3 ms during which time an input stimulus of randomized floating-point numbers will be generated at the adder input.

The simulation generates two text files: *ieee\_add\_in.txt* and *ieee\_add\_out.txt*. These files respectively contain the input and output data at the adder interfaces during the test.

## Synthesis

The source file 'ieee\_add.vhd' is the only file required for synthesis. There are no sub-modules in the design.

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx Virtex 5 and the Altera Stratix III series of FPGA devices. The lowest and highest speed grade devices have been chosen in both cases for comparison.

Resource usage is specified after Place and Route.

### VIRTEX 5

Resource type	Quantity used
Slice register	409
Slice LUT	749
Block RAM	0
DSP48	0
Clock frequency (worst case)	194 MHz
Clock frequency (best case)	281 MHz

### STRATIX III

Resource type	Quantity used
Register	290
ALUT	551
Block Memory bit	223
DSP block 18	0
Clock frequency (worse case)	178 MHz
Clock frequency (best case)	232 MHz

## Revision History

Revision	Change description	Date
1.0	Initial revision	30/04/2008