

Key Design Features

- Synthesizable, technology independent VHDL Core
- 32-bit floating-point arithmetic
- IEEE 754 compliant¹
- High-speed fully pipelined architecture
- Only 5 clock-cycles of latency

Applications

- Floating-point pipelines and arithmetic units
- Floating-point processors

Pin-out Description

Pin name	I/O	Description	Active state
clk	in	Synchronous clock	rising edge
en	in	Clock enable	high
v1 [31:0]	in	Input operand 1 in IEEE 754 format	data
v2 [31:0]	in	Input operand 2 in IEEE 754 format	data
vout [31:0]	out	Output result in IEEE 754 format	data

Functional Specification

Operand v1	Operand v2	Result
Standard IEEE	Standard IEEE	v1 + v2 If $ v1 + v2 > \text{MaxFloat}$ then result is: +/- Inf If $ v1 + v2 < \text{MinFloat}$ then result is: +/- 0
NaN	Anything	NaN
Anything	NaN	NaN
+/- Inf	- v1	NaN (e.g. -Inf + Inf)
+/- Inf	Standard IEEE	[sign(v1)] Inf

Block Diagram

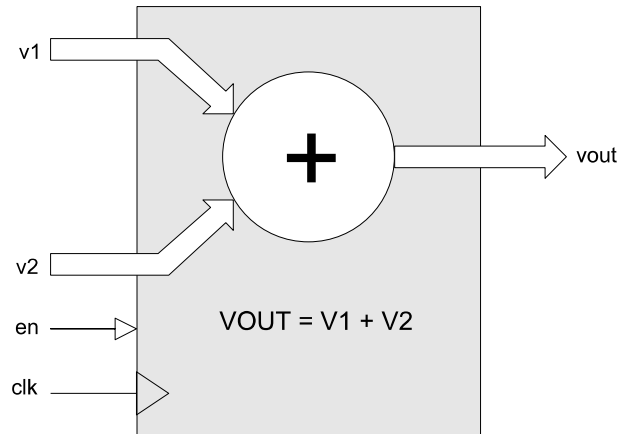


Figure 1: 32-bit Floating-point Adder

General Description

IEEE_ADD (Figure 1) is a high-speed fully pipelined 32-bit floating-point adder based on the IEEE 754 standard. The arrangement of the 32-bit floating-point number is summarized below:

MSB		LSB	
Sign (1-bit)	Exponent (8-bits)	Mantissa (23-bits)	

All input and output values comply with the IEEE 754 specification. The real number representation is calculated according to the formula:

$$Value = -1(S) * 2^{(E-127)} * 1.M$$

There are two exceptions to the IEEE 754 specification. The first being that denormalized numbers are treated as zero throughout the implementation, and the second being that symmetric arithmetic rounding is employed (round half-up).

Other points to note are that NaN is always generated as the value 0xFFC00000. The maximum floating-point value that may be represented is 0x7F7FFFFF or 0xFF7FFFFF (+/- MaxFloat). Likewise, the minimum floating-point value that may be represented is: 0x00800000 or 0x80800000 (+/- MinFloat). This means that a real number lies in the range:

$$2^{-126} \leq Value \leq 2^{127}(2-2^{-23})$$

All values are sampled on the rising clock-edge of *clk* when *en* is high. The function has a 5 clock-cycle latency².

1 Some minor features diverge from the IEEE 754 specification

2 The design may be optimized for higher-speed or lower latency on request. Please contact Zipcores.

Functional Timing

Figure 2 demonstrates the addition: $0x40010000 + 0x40407000 = 0x40A04000$ (or $2.0010 + 3.0068 = 5.0078$ in real numbers). The result has a latency of 5 clock cycles.

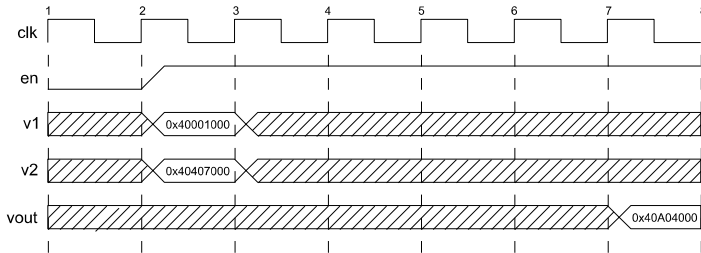


Figure 2: Addition of two floating-point numbers

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	Description
ieee_add.vhd	Top-level component
ieee_add_bench.vhd	Top-level test bench

Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. ieee_add.vhd
2. ieee_add_bench.vhd

The simulation must be run for at least 2 ms during which time an input stimulus of randomized floating-point numbers will be generated at the adder input.

The simulation generates two text files called: *ieee_add_in.txt* and *ieee_add_out.txt*. These files respectively contain the input and output floating-point numbers during the course of the test.

Synthesis

The source file 'ieee_add.vhd' is the only file required for synthesis. There are no sub-modules in the design.

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx Virtex 5 and the Altera Stratix III series of FPGA devices. The lowest and highest speed grade devices have been chosen in both cases for comparison.

Resource usage is specified after Place and Route.

VIRTEX 5

Resource type	Quantity used
Slice register	330
Slice LUT	729
Block RAM	0
DSP48	0
Clock frequency (worst case)	215 MHz
Clock frequency (best case)	275 MHz

STRATIX III

Resource type	Quantity used
Register	434
ALUT	537
Block Memory bit	0
DSP block 18	0
Clock frequency (worse case)	215 MHz
Clock frequency (best case)	282 MHz

Revision History

Revision	Change description	Date
1.0	Initial revision	30/04/2008
1.1	Updated synthesis results	20/08/2009
1.2	Updated functional specification. Updated synthesis results in line with minor code changes	19/09/2011