

Key Design Features

- Synthesizable, technology independent VHDL Core
- 16-bit signed output data samples
- 32-bit phase accumulator (tuning word)
- Phase resolution of $2\pi/2^{16}$
- Frequency resolution of $F_s/2^{32}$ (F_s = sample frequency)
- Phase dithering option for improved Spurious-Free Dynamic Range (SFDR)
- ≈ 100 dB Signal-to-Noise Ratio (SNR)
- > 110 dB SFDR (with phase dithering enabled)
- Simultaneous SIN, COS, Square and Sawtooth output waveforms
- Optimized quarter-wave LUT for reduced area footprint
- Sample rates of up to 300 MHz¹

Applications

- Digital oscillators
- Digital modulation
- Digital up/down conversion
- Generation of Quadrature (Complex) signals
- Versatile waveform generation

Pin-out Description

Pin name	I/O	Description	Active state
clk	in	Sample clock	rising edge
reset	in	Asynchronous reset	low
en	in	clock enable	high
phase_inc [31:0]	in	Phase increment as an unsigned 32-bit number (controls frequency of output waveform)	data
sin_out [15:0]	out	Sine wave output (16-bit signed number)	data
cos_out [15:0]	out	Cosine wave output (16-bit signed number)	data
squ_out [15:0]	out	Square wave output (16-bit signed number)	data
saw_out [15:0]	out	Sawtooth wave output (16-bit signed number)	data

¹ Altera Stratix III FPGA used as a benchmark

Block Diagram

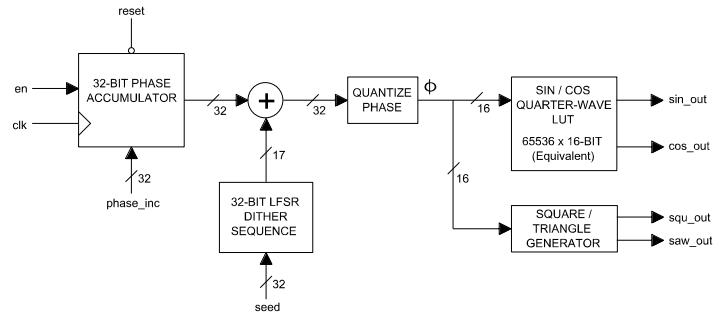


Figure 1: Direct Digital Synthesizer architecture

Generic Parameters

Generic name	Description	Type	Valid range
dithering	Enable phase dithering	boolean	TRUE/FALSE
seed	Seed for random number generator	std_logic vector	$0 < \text{seed} < 2^{32}$

General Description

DDS is a high-precision Direct Digital Synthesizer used for the generation of periodic waveforms. On each rising-edge of the sample clock, the phase in the phase accumulator is incremented by the value *phase_inc*. This phase is quantized to 16-bits and passed as an address to a look-up table which converts the phase into a waveform.

To save resources, the look-up table is implemented as a quarter sine wave (16384 x 15-bit samples). These samples are manipulated to generate 65536 x 16-bit samples over the range 0 to 2π . In addition to the quadrature outputs *sin_out* and *cos_out*, the DDS also provides square wave and sawtooth wave outputs: *squ_out* and *saw_out*. All output values are 16-bit signed numbers.

Phase increment

The frequency of the DDS output waveform is controlled by the phase increment on a clock-by-clock basis. A change in the phase increment during normal circuit operation will affect a change in the output waveform 5 sample clocks later. The phase increment may be calculated using the formula:

$$\Phi_{inc} = (F_{out} \cdot 2^{32}) / F_s + 0.5$$

Where F_{out} is the desired waveform output frequency and F_s is the sampling frequency. Note that the *integer* value of the phase increment must be used. As an example, consider a 100 MHz sample clock with a desired output frequency of 6.197 MHz. The phase increment would be calculated as $(6.197 \cdot 2^{32}) / 100 + 0.5 = 266159123$.

The minimum and maximum frequencies DDS can generate are given by the following formulas:

$$F_{min} = F_s / 2^{32} \quad , \quad F_{max} = F_s / 2$$

As an example, a 100 MHz sample clock would allow a minimum DDS frequency of 0.0233 Hz. This is sometimes called the frequency resolution of the DDS. Conversely, the maximum frequency the DDS can generate is given by the Nyquist/Shannon sampling theorem ($F_s/2$).

Phase dithering

The process of phase quantization introduces noise on the phase signal and it produces unwanted spurious spectral components in the DDS output signal (referred to as *spurs*). The difference between the carrier level and the maximum level of spurs is called the *Spurious Free Dynamic Range* (SFDR). The DDS component alleviates this problem by adding a 17-bit random number to the 32-bit phase accumulator before quantization. This has the effect of spreading the spurs throughout the available bandwidth, preventing spurs at the same harmonic frequencies reinforcing each other. With phase dithering enabled, an improvement of around 10 to 20 dB in SFDR may be achieved.

The random number used for phase dithering is generated using a *Linear Feedback Shift Register* (LFSR) of order 32. The LFSR is free running and generates a random bit every sample clock in accordance with the polynomial:

$$x^{32} + x^7 + x^5 + x^3 + x^2 + x^1 + x^0$$

The least significant 17-bits of the LFSR are added to the phase before quantization (See Figure 1). The user may choose any number (other than zero) as an initial seed for the random number generator. Different seeds, in some cases, can change the SFDR by around +/- 1dB.

Functional Timing

Figure 2 shows the operation of the DDS immediately after reset. After reset goes high the DDS starts to generate the output waveforms 5 clock cycles later. Asserting the clock-enable low will stall the pipeline. Asserting clock-enable high once again will reconvene waveform output at the next sample point on the waveform.

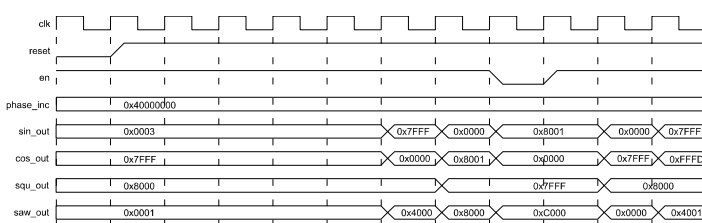


Figure 2: DDS operation after reset

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	Description
sincos_lut.vhd	SIN/COS look-up table
dds.vhd	Top-level block
dds_bench.vhd	Top-level test bench

Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. sincos_lut.vhd
2. dds.vhd
3. dds_bench.vhd

The VHDL testbench instantiates the DDS component and the user may modify the phase increment and generic parameters in order to generate the desired output waveform. The example provided generates a 2.73 MHz waveform with a 100 MHz sample clock.

The simulation must be run for at least 3 ms during which time the DDS will output the SIN, COS, square and sawtooth waveforms. Output samples are captured in the text file *dds_out.txt*. Figures 3 to 6 show plots of the resulting waveforms.

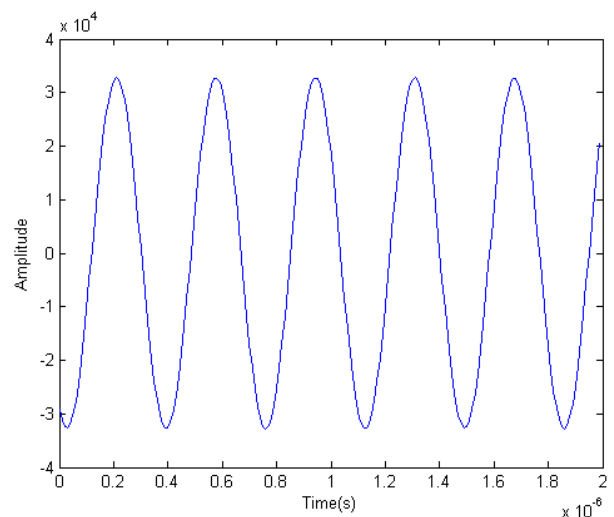


Figure 3: SIN waveform output (2.73 MHz)

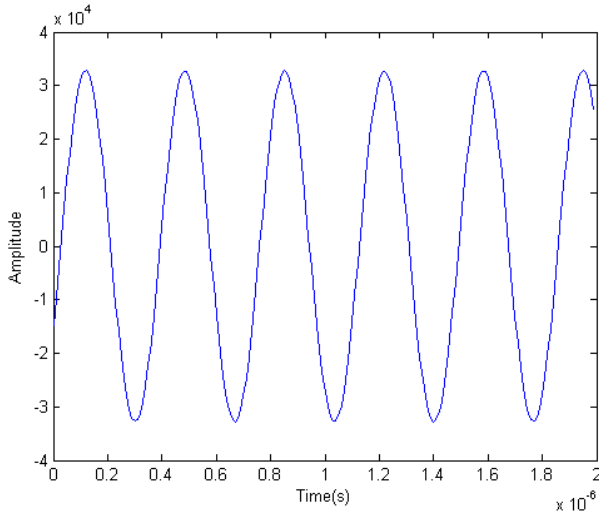


Figure 4: COS waveform output (2.73 MHz)

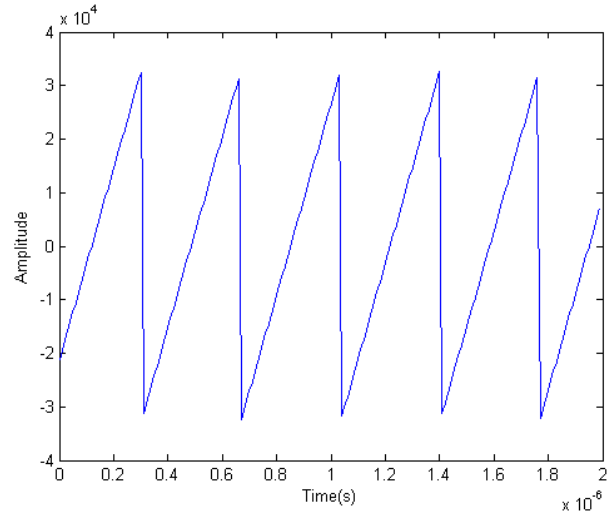


Figure 6: Sawtooth waveform output (2.73 MHz)

Performance

The following plots demonstrate the effect of phase dithering on the output power spectra. The plots show the mean-squared power estimate of the SIN output samples for a 100MHz sample clock and a 2.73 MHz output waveform:

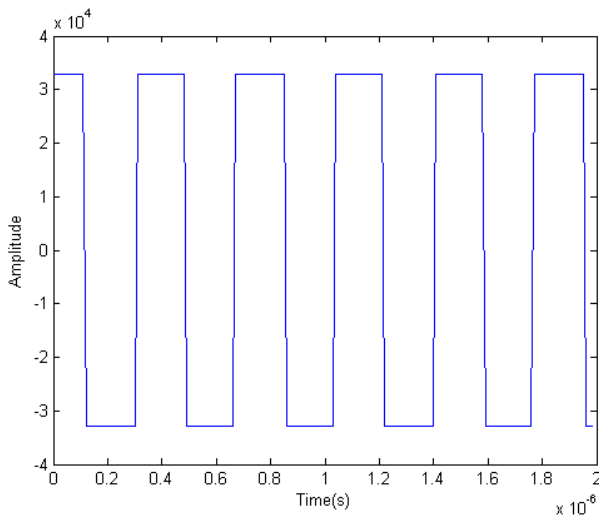


Figure 5: Square waveform output (2.73 MHz)

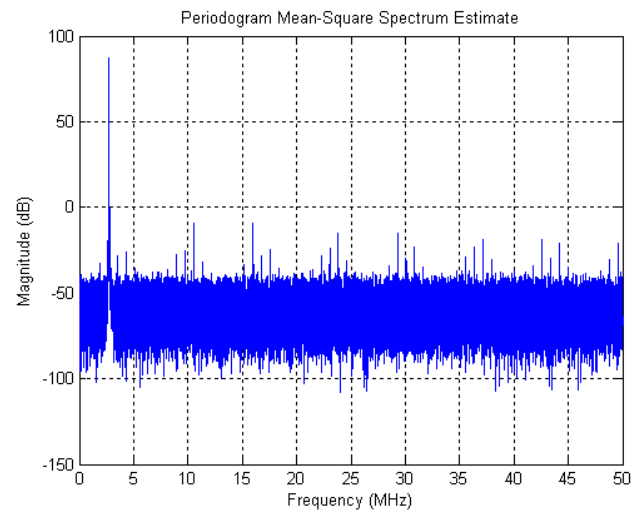


Figure 7: Single 2.73 MHz tone - dithering disabled

The SFDR for the non phase-dithered case (Figure 7) exhibits an SFDR of 96.3 dB with the largest magnitude spur of -9.1 dB at around 16 MHz.

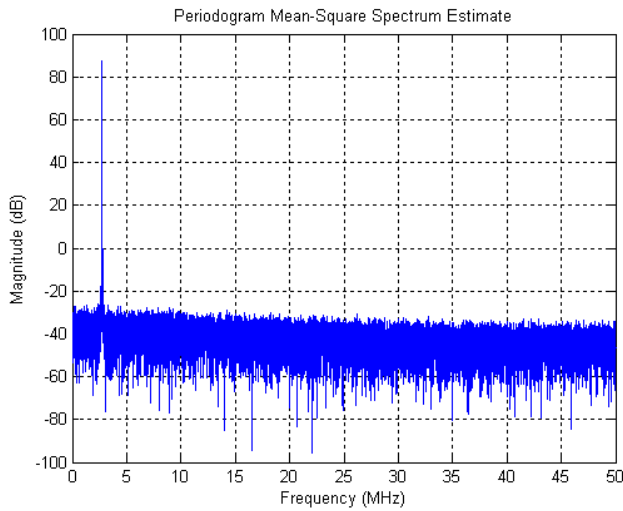


Figure 8: Single 2.73 MHz tone - dithering enabled

Figure 8 shows the same 2.73 MHz tone with phase-dithering enabled. The SFDR is 114.9 dB with the largest magnitude spur of -27.7 dB at around 8 MHz. This is an improvement in SFDR of 18.6 dB.

Synthesis

The files required for synthesis and the design hierarchy is shown below:

- dds.vhd
- sincos_lut.vhd

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx Virtex 5 and the Altera Stratix III series of FPGA devices. The lowest and highest speed grade devices have been chosen in both cases for comparison.

Trial synthesis results are shown with the generic parameters set to: dithering = true, seed = 0x7AF1093D.

Resource usage is specified after Place and Route.

VIRTEX 5

Resource type	Quantity used
Slice register	164
Slice LUT	194
Block RAM	15
DSP48	0
Clock frequency (worst case)	176 MHz
Clock frequency (best case)	233 MHz

STRATIX III

Resource type	Quantity used
Register	164
ALUT	178
Block Memory bit	491520
DSP block 18	0
Clock frequency (worse case)	242 MHz
Clock frequency (best case)	300 MHz

Revision History

Revision	Change description	Date
1.0	Initial revision	22/05/2008
1.1	Modified key design features	06/11/2008