Key Design Features

- Synthesizable, technology independent VHDL Core
- Function φ = atan2 (y,x)
- Inputs as 12-bit signed numbers
- Output phase as a 19-bit signed
- Output range -π ≤ φ ≤ π
- Accurate to within 0.00008 radians
- High-speed fully pipelined architecture
- Small implementation size
- 7 clock-cycle latency

Applications

- Fixed-point mathematics
- Precision phase measurements in digital communications and digital signal processing
- Digital Phase-locked Loops (PLLs)
- More accurate, smaller, lower latency and faster than a CORDIC solution of similar specification

Pin-out Description

Pin name	*I/O*	*Description*	*Active state*
clk	in	Synchronous clock	rising edge
en	in	Clock enable	high
x_in [11:0]	in	Input value	data
y_in [11:0]	in	Input value	data
phi_out [18:0]	out	Output phase angle in radians	data

Functional Specification

Value	*Type*	*Valid range*
x_in [11:0]	12-bit signed number	[-2048, 2047]
y_in [11:0]	12-bit signed number	[-2048, 2047]
phi_out [18:0]	19-bit signed fraction in [19 16] format	[-π, π] Accurate to within 0.00008 radians

Block Diagram

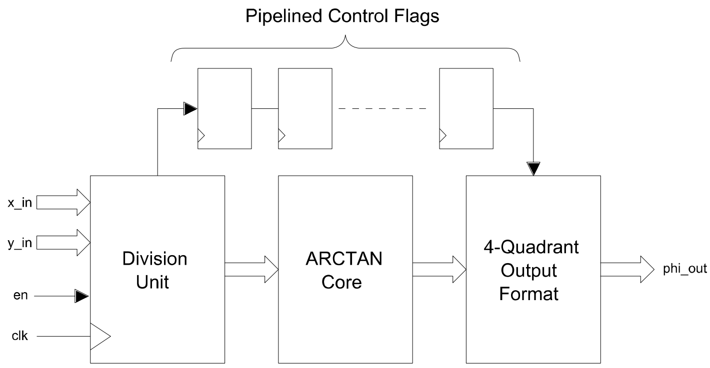

Figure 1: 4-quadrant Arctan core architecture

General Description

ATAN2_XY (Figure 1) calculates the 4-quadrant inverse tangent in the range -π to π. It has a fully pipelined architecture and uses fixed-point mathematics throughout. Input values are accepted as 12-bit signed numbers in the range -2048 to 2047. The calculated output phase (in radians) is a 19-bit signed value with 1 sign bit, 2 integer bits and 16 fractional bits. As an example, the output phase angle 0x18000 would represent 1.5 radians and the value 0x68000 would represent the value -1.5 radians. Internally, the arctan core function uses a 2nd order polynomial of the form:

$$y = ax^2 + bx + c$$

The coefficients a, b and c dynamically change with respect to the input value in order to generate a more accurate approximation. The output result is accurate to within 0.00008 radians.

Values are sampled on the rising clock-edge of *clk* when *en* is high. The function has a 7 clock-cycle latency.

Functional Timing

Figure 2 demonstrates a series of computations of φ = atan2 (y,x). Samples are processed on the rising edge of *clk* when *en* is high. The function has a 7 cycle latency as shown by the timing between edges 'A' and 'B' in the waveform.

In the example, the first calculation is φ = atan2(0x02C,0x07E), the next calculation is φ = atan2(0xEB7, 0x98D). The results are respectively 0x05601 and 0x50E1B. Converting the numbers to decimals and decimal fractions the calculations are equivalent to:

$$\varphi = atan2\,(44,126) = 0.335953$$

and ..

$$\varphi = atan2\,(-329,-1651) = -2.944901$$

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Note that the clock-enable is held low for one clock cycle during the second sample during which the whole pipeline is stalled.

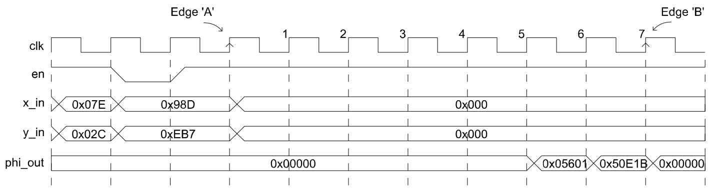

Figure 2: Timing waveform for the atan2_xy function

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	***Description***
lut_reciprocal.vhd	Reciprocal unit
lut_divide.vhd	Division unit
atan_x.vhd	Arctan core function
atan2_xy.vhd	Top-level block
atan2_xy_bench.vhd	Top-level test bench

Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. lut_reciprocal.vhd
2. lut_divide.vhd
3. atan_x.vhd
4. atan2_xy.vhd
5. atan2_xy_bench.vhd

The simulation must be run for at least 2 ms during which time a randomized 2 x 12-bit input stimulus will be generated at the input to the arctan core. The test terminates automatically.

The simulation generates two text files called *atan2_xy_in.txt* and *atan2_xy_out.txt*. These files contain the input and output samples captured during the course of the test and may be used to verify the correct operation of the core.

Performance

Quadrature samples were generated in the range -π to π in order to check the accuracy and linearity of the phase output. Quadrature samples were generated according to the formulas:

$$x = G * \cos(\varphi)$$
$$y = G * \sin(\varphi)$$

Where φ is a phase angle in the range [-π, π] and G is a scale factor. The generated x, y samples were used as an input stimulus to the ATAN2_XY core and the output samples were captured during the simulation.

Figure 3 shows the resulting plot of (ideal) input phase vs. output phase in radians. The overall accuracy was measured at 0.00008 radians. This compares with a theoretical best case of 0.000015 radians for a 16-bit fractional output.

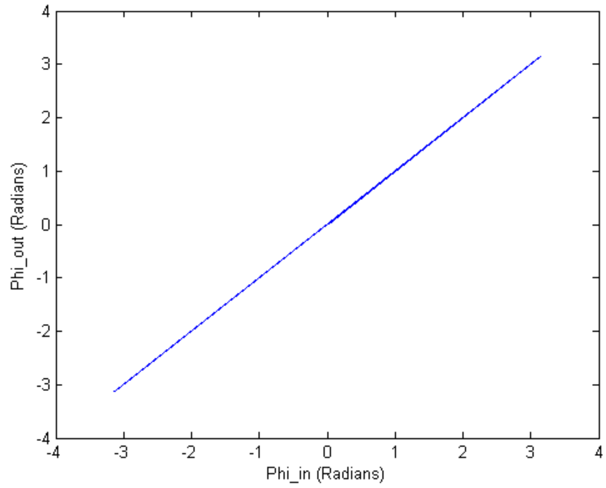

Figure 3: Plot of Input phase vs. output phase showing good linear relationship

Synthesis

The source files required for synthesis and the design hierarchy is shown below:

- atan2_xy.vhd
  - lut_reciprocal.vhd
  - lut_divide.vhd

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx Virtex 5 and the Altera Stratix III series of FPGA devices. The lowest and highest speed grade devices have been chosen in both cases for comparison.

Note that in order to reduce cycle latency, the division unit has been implemented using a ROM-based LUT. As a result, the design uses a significant proportion of the Block RAM resource on smaller FPGA devices[1].

Resource usage is specified after Place and Route.

1 Contact ZIPcores for alternative division algorithms that target core logic as opposed to Block-RAM resource

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VIRTEX 5

Resource type	***Quantity used***
Slice register	33
Slice LUT	387
Block RAM	4
DSP48	4
Clock frequency (worst case)	110 MHz
Clock frequency (best case)	155 MHz

STRATIX III

Resource type	***Quantity used***
Register	121
ALUT	384
Block Memory bit	98304
DSP block 18	10
Clock frequency (worse case)	130 MHz
Clock frequency (best case)	167 MHz

Revision History

Revision	***Change description***	***Date***
1.0	Initial revision	28/04/09

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